Search History

STN
(HCAPLUS, INSPEC, JAPIO, USPATALL)
1/19/05

=> d l11 1-6 abs,bib

L11 ANSWER 1 OF 6 USPATFULL on STN
AB An apparatus and method for forming an epitaxial layer on and a denuded zone in a semiconductor wafer. A single chamber is used to form both the epitaxial layer and the denuded zone. The denuded zone is formed by heating the wafer in the chamber and then rapidly cooling the wafer while it is supported on an annular support whereby only a peripheral edge portion of the wafer is in contact with the support.

AN 2003:203278 USPATFULL
TI Method and apparatus for forming a silicon wafer with a denuded zone
IN Yang, Charles Chiun-Chieh, St. Peters, MO, United States
PA MEMC Electronic Materials, Inc., St. Peters, MO, United States (U.S. corporation)
PI US 6599815 B1 20030729
AI US 2000-607391 20000630 (9)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Mulpuri, Savitri
LREP Senniger, Powers, Leavitt & Roedel
CLMN Number of Claims: 17
ECL Exemplary Claim: 1
DRWN 9 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 928

L11 ANSWER 2 OF 6 USPATFULL on STN
AB An apparatus and method are provided for forming a denuded zone and an epitaxial layer on a semiconductor wafer used in manufacturing electronic components. The denuded zone and epitaxial layer are formed in one chamber. The apparatus includes a plurality of upstanding pins immovably mounted on a susceptor and maintain a semiconductor wafer spaced from the susceptor during both application of the epitaxial layer and formation of the denuded zone. Fast cooling of the wafer is accomplished by having the wafer out of conductive heat transfer relation with the susceptor during cooling thereof.

AN 2002:154317 USPATFULL
TI Apparatus for forming an epitaxial silicon wafer with a denuded zone
IN Torack, Tom, Oakland, MO, UNITED STATES
Ries, Michael J., St. Charles, MO, UNITED STATES
PA MEMC Electronic Materials Inc. (U.S. corporation)
PI US 2002078882 A1 20020627
AI US 2002-50026 A1 20020115 (10)
RLI Division of Ser. No. US 2000-607389, filed on 30 Jun 2000, GRANTED, Pat. No. US 6339016
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102
CLMN Number of Claims: 3
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 845

L11 ANSWER 3 OF 6 USPATFULL on STN
AB An apparatus and method are provided for forming a denuded zone and an epitaxial layer on a semiconductor wafer used in manufacturing electronic components. The denuded zone and epitaxial layer are formed in one chamber. The apparatus includes a plurality of upstanding pins immovably mounted on a susceptor and maintain a semiconductor wafer spaced from the susceptor during both application of the epitaxial layer and formation of the denuded zone. Fast cooling of the wafer is

accomplished by having the wafer out of conductive heat transfer relation with the susceptor during cooling thereof.

AN 2002:9805 USPATFULL
TI Method and apparatus for forming an epitaxial silicon wafer with a denuded zone
IN Torack, Tom, Oakland, MO, United States
Ries, Michael John, St. Charles, MO, United States
PA MEMC Electronic Materials, Inc., St. Peters, MI, United States (U.S. corporation)
PI US 6339016 B1 20020115
AI US 2000-607389 20000630 (9)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Nelms, David; Assistant Examiner: Dang, Phuc T.
LREP Senniger, Powers, Leavitt & Roedel
CLMN Number of Claims: 18
ECL Exemplary Claim: 1
DRWN 5 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 934

L11 ANSWER 4 OF 6 USPATFULL on STN
AB This invention is directed to a novel a single crystal silicon wafer. In one embodiment, this wafer comprises: (a) two major generally parallel surfaces (i.e., the front and back surfaces); (b) a central plane between and parallel to the front and back surfaces; (c) a front surface layer which comprises the region of the wafer extending a distance of at least about 10 μm from the front surface toward the central plane; and (d) a bulk layer which comprises the region of the wafer extending from the central plane to the front surface layer. This wafer is characterized in that the wafer has a non-uniform distribution of crystal lattice vacancies, wherein (a) the concentration of crystal lattice vacancies in the bulk layer are greater than the concentration of crystal lattice vacancies in the front surface layer, (b) the crystal lattice vacancies have a concentration profile in which the peak density of the crystal lattice vacancies is at or near the central plane, and (c) the concentration of crystal lattice vacancies generally decreases from the position of peak density toward the front surface of the wafer. In addition, the front surface of the wafer has an epitaxial layer deposited thereon. This epitaxial layer has a thickness of from about 0.1 to about 2.0 μm.

This invention is also directed to a novel process for the preparation of a silicon wafer comprising a surface having an epitaxial layer deposited thereon. In one embodiment, the process comprises heating a surface of a wafer starting material to remove a silicon oxide layer from the surface. Within about 30 seconds after removing the silicon oxide layer from the surface, the surface is exposed to an atmosphere comprising silicon to deposit a silicon epitaxial layer onto the surface to form an epitaxial wafer. The epitaxial wafer is then heated to a soak temperature of at least about 1175° C. while exposing the epitaxial layer to an oxidizing atmosphere comprising an oxidant. Afterwards, the heated epitaxial wafer is cooled at a rate of at least about 10° C./sec.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:186955 USPATFULL
TI Epitaxial silicon wafer with intrinsic gettering and a method for the preparation thereof
IN Wilson, Gregory M., Chesterfield, MO, United States
Rossi, Jon A., Chesterfield, MO, United States
Yang, Charles C., St. Peters, MO, United States
PI US 2001032581 A1 20011025

US 6537655 B2 20030325
AI US 2001-859094 A1 20010516 (9)
RLI Division of Ser. No. US 1999-250908, filed on 16 Feb 1999, GRANTED, Pat. No. US 6284384
PRAI US 1998-111546P 19981209 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102
CLMN Number of Claims: 58
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 1449
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L11 ANSWER 5 OF 6 USPATFULL on STN
AB This invention is directed to a novel a single crystal silicon wafer. The wafer comprises: (a) two major generally parallel surfaces (ie., the front and back surfaces); (b) a central plane between and parallel to the front and back surfaces; (c) a front surface layer which comprises the region of the wafer extending a distance of at least about 10 μm from the front surface toward the central plane; and (d) a bulk layer which comprises the region of the wafer extending from the central plane to the front surface layer. This wafer is characterized in that the wafer has a non-uniform distribution of crystal lattice vacancies, wherein (a) the concentration of crystal lattice vacancies in the bulk layer are greater than the concentration of crystal lattice vacancies in the front surface layer, (b) the crystal lattice vacancies have a concentration profile in which the peak density of the crystal lattice vacancies is at or near the central plane, and (c) the concentration of crystal lattice vacancies generally decreases from the position of peak density toward the front surface of the wafer. In addition, the front surface of the wafer has an epitaxial layer deposited thereon. The epitaxial layer has an average light scattering event concentration of no greater than about 0.06/cm.sup.2 as measured by a laser-based auto inspection tool configured to detect light scattering events corresponding to polystyrene spheres having diameters of no less than about 0.12 μm. The bulk layer comprises voids which are at least about 0.01 μm in their largest dimension.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:147598 USPATFULL
TI Epitaxial silicon wafer with intrinsic gettering
IN Wilson, Gregory M., Chesterfield, MO, United States
Rossi, Jon A., Chesterfield, MO, United States
Yang, Charles C., St. Peters, MO, United States
PA MEMC Electronic Materials, Inc., St. Peters, MO, United States (U.S. corporation)
PI US 6284384 B1 20010904
AI US 1999-250908 19990216 (9)
PRAI US 1998-111546P 19981209 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Jones, Deborah; Assistant Examiner: Stein, Stephen
LREP Senniger, Powers, Leavitt & Roedel
CLMN Number of Claims: 7
ECL Exemplary Claim: 1
DRWN 8 Drawing Figure(s); 4 Drawing Page(s)
LN.CNT 1206
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L11 ANSWER 6 OF 6 USPAT2 on STN
AB This invention is directed to a novel a single crystal silicon wafer. In

one embodiment, this wafer comprises: (a) two major generally parallel surfaces (i.e., the front and back surfaces); (b) a central plane between and parallel to the front and back surfaces; (c) a front surface layer which comprises the region of the wafer extending a distance of at least about 10 μm from the front surface toward the central plane; and (d) a bulk layer which comprises the region of the wafer extending from the central plane to the front surface layer. This wafer is characterized in that the wafer has a non-uniform distribution of crystal lattice vacancies, wherein (a) the concentration of crystal lattice vacancies in the bulk layer are greater than the concentration of crystal lattice vacancies in the front surface layer, (b) the crystal lattice vacancies have a concentration profile in which the peak density of the crystal lattice vacancies is at or near the central plane, and (c) the concentration of crystal lattice vacancies generally decreases from the position of peak density toward the front surface of the wafer. In addition, the front surface of the wafer has an epitaxial layer deposited thereon. This epitaxial layer has a thickness of from about 0.1 to about 2.0 μm.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:186955 USPAT2
TI Epitaxial silicon wafer with intrinsic gettering and a method for the preparation thereof
IN Wilson, Gregory M., Chesterfield, MO, United States
Rossi, Jon A., Chesterfield, MO, United States
Yang, Charles C., St. Peters, MO, United States
PA MEMC Electronic Materials, Inc., St. Peters, MO, United States (U.S. corporation)
PI US 6537655 B2 20030325
AI US 2001-859094 20010516 (9)
RLI Division of Ser. No. US 1999-250908, filed on 16 Feb 1999, now patented, Pat. No. US 6284384, issued on 4 Sep 2001
PRAI US 1998-111546P 19981209 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Kunemund, Robert
LREP Senniger, Powers, Leavitt & Roedel
CLMN Number of Claims: 6
ECL Exemplary Claim: 1
DRWN 8 Drawing Figure(s); 4 Drawing Page(s)
LN.CNT 1140
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

=> d his

(FILE 'HOME' ENTERED AT 09:32:15 ON 19 JAN 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 09:32:26 ON 19 JAN 2005

L1 118 S (CZ OR CZOCHRALSKI)(10A)(COOL?(6A)RATE#)
L2 751040 S (VARY? OR ALTER? OR MEASUR? OR CONTROL?)(8A)(TEMPERATURE#)
L3 748419 S (VARY? OR ALTER? OR CONTROL? OR MEASUR? OR ADJUST?)(8A)(TEMPE
L4 159253 S (ERROR(8A)SIGNAL#)
L5 177819 S (POST OR AFTER)(10A)(GROW? OR PROCESS)
L6 417943 S (TEMPERATURE(8A)COOL? OR TEMPERATUR(8A)COOL?(2W)RATE#)
L7 29931 S (SINGLE(W)CRYSTA? OR MONOCRYSTAL?)(8A)(PULL? OR LIFT? OR PROD
L8 0 S L2 AND L3 AND L4 AND L5 AND L6 AND L7
L9 1472 S L2 AND L3 AND L6 AND L7
L10 36 S L1 AND L9
L11 6 S L5 AND L10

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Search History

STN
(USPATALL, INSPEC, JAPIO, HCAPLUS)
1/19/05

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=> d his

     (FILE 'HOME' ENTERED AT 06:51:39 ON 19 JAN 2005)

     FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 06:51:56 ON
     19 JAN 2005
L1          5820 S (SINGEL OR MONO)(8A)(CRYSTAL?)
L2        175787 S (FIRST OR PRIMARY)(8A)(TEMPERATURE(6A)SENSOR# OR TEMPERATURE)
L3        184255 S (SECOND?)(8A)(TEMPERATURE(6A)SENSOR# OR TEMPERATURE)
L4         96595 S (COOL?(4A)RATE#)
L5       1964004 S (DISTANCE#)
L6        456404 S (FIRST(6A)POSITION#)
L7        427147 S (SECOND?(6A)POSITION#)
L8         39041 S (CZ OR CZOCHRALSKI)
L9           397 S (COOL?(4A)RATE#)(8A)(MONOCRYSTAL? OR SINGLE(W)CRYSTAL?)

=> s l1 and l2 and l3 and l5 and l8 and l9
L10           0 L1 AND L2 AND L3 AND L5 AND L8 AND L9

=> s l1 and l2 and l3
L11         173 L1 AND L2 AND L3

=> s l1 and l2 and l3 and l9
L12           0 L1 AND L2 AND L3 AND L9

=> s l1 and l2 and l3 and l4
L13          27 L1 AND L2 AND L3 AND L4

=> s l1 and l2 and l3 and l4 and l5
L14          13 L1 AND L2 AND L3 AND L4 AND L5

=> s l1 and l2 and l3 and l4 and l5 and l8
L15           0 L1 AND L2 AND L3 AND L4 AND L5 AND L8

=> d l14 1-13 abs,bib

L14  ANSWER 1 OF 13  USPATFULL on STN
AB     To provide a method of improving the characteristics and reliability of
       thin film transistors (TFT) which have been formed with a highest
       process temperature of not more than 700° C. Crystalline silicon
       films are thermally oxidized and TFT gate insulating films, for example,
       are formed with the oxide so obtained. At this time, the thermal
       oxidation is carried out at a temperature of 500-700° C. in such
       a way that no thermal damage is done to the substrate, for example, and
       a reactive gas which contains thermally excited or decomposed oxygen or
       nitrogen oxide (NO.sub.X, where 0.5≤+≤2.5) is used
       for the oxidizing gas. The oxidation reaction may be promoted by heating
       in an atmosphere of oxides of nitrogen at a high pressure of 2-10
       atmospheres. Deterioration due to the implantation of hot electrons, for
       example, can be prevented and element reliability can be increased by
       using the thermal oxide films obtained in this way as gate insulating
       films.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN     2004:65919  USPATFULL
TI     Method for manufacturing a thin film transistor using a high pressure
       oxidation step
IN     Yamazaki, Shunpei, Tokyo, JAPAN
       Takemura, Yasuhiko, Kanagawa, JAPAN
PA     Semiconductor Energy Laboratory Co., Ltd., Kanagawa-ken, JAPAN (non-U.S.
       corporation)
PI     US 6706572          B1   20040316
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AI US 2000-615078 20000712 (9)
RLI Division of Ser. No. US 1995-521532, filed on 30 Aug 1995, now patented, Pat. No. US 6150203
PRAI JP 1994-232409 19940831
DT Utility
FS GRANTED
EXNAM Primary Examiner: Wilczewski, Mary
LREP Robinson, Eric J., Robinson Intellectual Property Law Office, P.C.
CLMN Number of Claims: 23
ECL Exemplary Claim: 1
DRWN 24 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 1109
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L14 ANSWER 2 OF 13 USPATFULL on STN
AB The invention relates to a meltable ink which is solid at room temperature, which ink is suitable for use in an indirect printing process, in which printing process the ink is transferred, by the use of an inkjet printhead, to a transfer element, whereafter the ink is transferred to a receiving material under pressure from the transfer element, the ink having a composition such that it is pressure-transferable at a temperature between a bottom limit and a top limit, wherein the ink has a deformation energy of less than 20+10.sup.5 Pa.s at a temperature equal to said top limit.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:29619 USPATFULL
TI Meltable ink for an inkjet printer and a method of selecting such an ink
IN Kremers, Martinus Antonius, Ottersum, NETHERLANDS
Thijssen, Maurice Hendrikus Hubertinus, Deurne, NETHERLANDS
Weitenauer, Berby Marga Gerarda, Venlo, NETHERLANDS
PI US 2004021754 A1 20040205
AI US 2003-611877 A1 20030703 (10)
PRAI NL 2002-1021011 20020705
DT Utility
FS APPLICATION
LREP BIRCH STEWART KOLASCH & BIRCH, PO BOX 747, FALLS CHURCH, VA, 22040-0747
CLMN Number of Claims: 9
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 772
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L14 ANSWER 3 OF 13 USPATFULL on STN
AB A method of manufacturing a ferrodielectric liquid crystal display device includes the steps of injecting melted ferrodielectric liquid crystal in a cell formed between a lower structure body and an upper structure body each having a substrate, an electrode layer, and an orientation film and sealing the cell; cooling to obtain phase transitions of the ferrodielectric liquid crystal corresponding to a bookshelf structure; applying dc potentials to the electrode layers at temperatures ranging from temperatures higher than phase transition temperatures to temperatures lower than phase transition temperatures, stopping the dc potential applications and cooling until below a predetermined temperature, and applying a reverse potential to the electrode layers and cooling again. The ferrodielectric liquid crystal display device produced by such a manufacturing method can display clear black-and-white states with the liquid **crystal** layers having a **mono** domain of the bookshelf structure.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:11802 USPATFULL
TI Ferrodielectric liquid crystal display (FLCD) manufacturing method

IN Wang, Jong-min, Seoul, KOREA, REPUBLIC OF
Kim, Chang-ju, Gyunggi-do, KOREA, REPUBLIC OF
PA SAMSUNG ELECTRONICS CO., LTD. (non-U.S. corporation)
PI US 2004008315 A1 20040115
US 6844909 B2 20050118
AI US 2003-403521 A1 20030401 (10)
PRAI KR 2002-18086 20020402
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 Pennsylvania Avenue, NW, Washington, DC, 20037-3213
CLMN Number of Claims: 5
ECL Exemplary Claim: 1
DRWN 6 Drawing Page(s)
LN.CNT 443
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L14 ANSWER 4 OF 13 USPATFULL on STN
AB A method and apparatus for axially growing single crystal silicon carbide is provided. Utilizing the system, silicon carbide can be grown with a dislocation density of less than 10.sup.4 per square centimeter, a micropipe density of less than 10 per square centimeter, and a secondary phase inclusion density of less than 10 per cubic centimeter. As disclosed, a SiC source and a SiC seed crystal of the desired polytype are co-located within a crucible, the growth zone being defined by the substantially parallel surfaces of the source and the seed in combination with the sidewalls of the crucible. Prior to reaching the growth temperature, the crucible is evacuated and sealed, either directly or through the use of a secondary container housing the crucible. The crucible is comprised of tantalum or niobium that has been specially treated. As a result of the treatment, the inner surfaces of the crucible exhibit a depth variable composition of Ta--Si--C or Nb--Si--C that is no longer capable of absorbing SiC vapors, thus allowing the vapor-phase composition within the crucible to be close to the SiC--Si system with the partial pressure of Si-vapor slightly higher than that in the SiC--Si system.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:162313 USPATFULL
TI Tantalum crucible fabrication and treatment
IN Vodakov, Yury Alexandrovich, St. Petersburg, RUSSIAN FEDERATION
Mokhov, Evgeny Nikolaevich, St Petersburg, RUSSIAN FEDERATION
Ramm, Mark Grigorievich, Rego Park, NY, UNITED STATES
Roenkov, Alexandr Dmitrievich, St. Petersburg, RUSSIAN FEDERATION
Makarov, Yury Nikolaevich, Richmond, VA, UNITED STATES
Karpov, Sergei Yurievich, St. Petersburg, RUSSIAN FEDERATION
Ramm, Mark Spiridonovich, St. Petersburg, RUSSIAN FEDERATION
Temkin, Leonid Iosifovich, St. Petersburg, RUSSIAN FEDERATION
PI US 2002083890 A1 20020704
US 6547877 B2 20030415
AI US 2001-849767 A1 20010504 (9)
RLI Continuation-in-part of Ser. No. US 1999-355561, filed on 20 Jul 1999, GRANTED, Pat. No. US 6261363 A 371 of International Ser. No. WO 1997-RU5, filed on 22 Jan 1997, UNKNOWN
DT Utility
FS APPLICATION
LREP David G. Beck, Esq., McCutchen, Doyle, Brown & Enersen, Three Embarcadero Center, San Francisco, CA, 94111-2286
CLMN Number of Claims: 34
ECL Exemplary Claim: 1
DRWN 1 Drawing Page(s)
LN.CNT 558
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L14 ANSWER 5 OF 13 USPATFULL on STN

AB A method and apparatus for axially growing single crystal silicon carbide is provided. Utilizing the system, silicon carbide can be grown with a dislocation density of less than 10.sup.4 per square centimeter, a micropipe density of less than 10 per square centimeter, and a secondary phase inclusion density of less than 10 per cubic centimeter. As disclosed, a SiC source and a SiC seed crystal of the desired polytype are co-located within a crucible, the growth zone being defined by the substantially parallel surfaces of the source and the seed in combination with the sidewalls of the crucible. Prior to reaching the growth temperature, the crucible is evacuated and sealed, either directly or through the use of a secondary container housing the crucible. The crucible is comprised of tantalum or niobium that has been specially treated. As a result of the treatment, the inner surfaces of the crucible exhibit a depth variable composition of Ta--Si--C or Nb--Si--C that is no longer capable of absorbing SiC vapors, thus allowing the vapor-phase composition within the crucible to be close to the SiC--Si system with the partial pressure of Si-vapor slightly higher than that in the SiC--Si system.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:117934 USPATFULL

TI Niobium crucible fabrication and treatment

IN Vodakov, Yury Alexandrovich, St. Petersburg, RUSSIAN FEDERATION
Mokhov, Evgeny Nikolaevich, St Petersburg, RUSSIAN FEDERATION
Ramm, Mark Grigorievich, Rego Park, NY, UNITED STATES
Roenkov, Alexandr Dmitrievich, St. Petersburg, RUSSIAN FEDERATION
Makarov, Yury Nikolaevich, Richmond, VA, UNITED STATES
Karpov, Sergei Yurievich, St. Petersburg, RUSSIAN FEDERATION
Ramm, Mark Spiridonovich, St Petersburg, RUSSIAN FEDERATION
Temkin, Leonid Iosifovich, St. Petersburg, RUSSIAN FEDERATION

PI US 2002059902 A1 20020523
US 6537371 B2 20030325

AI US 2001-849766 A1 20010504 (9)

RLI Continuation-in-part of Ser. No. US 1999-355561, filed on 20 Jul 1999, PATENTED

PRAI WO 1997-RU5 19970122

DT Utility

FS APPLICATION

LREP David G. Beck, Esq., McCutchen, Doyle, Brown & Enersen, Three Embarcadero Center, San Francisco, CA, 94111-2286

CLMN Number of Claims: 34

ECL Exemplary Claim: 1

DRWN 1 Drawing Page(s)

LN.CNT 558

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L14 ANSWER 6 OF 13 USPATFULL on STN

AB To provide a method of improving the characteristics and reliability of thin film transistors (TFT) which have been formed with a highest process temperature of not more than 700° C. Crystalline silicon films are thermally oxidized and TFT gate insulating films, for example, are formed with the oxide so obtained. At this time, the thermal oxidation is carried out at a temperature of 500-700° C. in such a way that no thermal damage is done to the substrate, for example, and a reactive gas which contains thermally excited or decomposed oxygen or nitrogen oxide (NO.sub.X, where $0.5 \leq + \leq 2.5$) is used for the oxidizing gas. The oxidation reaction may be promoted by heating in an atmosphere of oxides of nitrogen at a high pressure of 2-10 atmospheres. Deterioration due to the implantation of hot electrons, for example, can be prevented and element reliability can be increased by using the thermal oxide films obtained in this way as gate insulating

films.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2000:157256 USPATFULL
TI Method for manufacturing a semiconductor device
IN Yamazaki, Shunpei, Tokyo, Japan
Takemura, Yasuhiko, Kanagawa, Japan
PA Semiconductor Energy Laboratory Co., Ltd., Kanagawa-ken, Japan (non-U.S. corporation)
PI US 6150203 20001121
AI US 1995-521532 19950830 (8)
PRAI JP 1994-232409 19940831
DT Utility
FS Granted
EXNAM Primary Examiner: Bowers, Charles; Assistant Examiner: Kielin, Erik J
LREP Robinson, Eric J.Nixon Peabody LLP
CLMN Number of Claims: 28
ECL Exemplary Claim: 10
DRWN 24 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 1083
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L14 ANSWER 7 OF 13 USPATFULL on STN
AB A semiconductor device comprising a semiconductor body having a depression formed into the first surface of the body. The device further comprises member means comprising a thermal-to-electric transducer or static electric element, the member means having a predetermined configuration suspended over the depression. The member means is connected to the first surface so that the predetermined configuration is cantilevered over the depression, the depression opening to the first surface around at least a portion of the predetermined configuration. The depression provides substantial physical and thermal isolation between the element and the semiconductor body. In this manner, an integrated semiconductor device provides an environment of substantial physical and thermal isolation between the transducer or element and the semiconductor body.

AN 90:82763 USPATFULL
TI Cantilever semiconductor device
IN Sumner, John P., Edina, MN, United States
Johnson, Robert G., Minnetonka, MN, United States
Higashi, Robert E., Minneapolis, MN, United States
PA Honeywell Inc., Minneapolis, MN, United States (U.S. corporation)
PI US 4966037 19901030
AI US 1985-782188 19851001 (6)
DCD 20050130
RLI Continuation of Ser. No. US 1983-531130, filed on 12 Sep 1983, now abandoned
DT Utility
FS Granted
EXNAM Primary Examiner: Goldstein, Herbert
LREP Bruns, Gregory A.
CLMN Number of Claims: 59
ECL Exemplary Claim: 1
DRWN 13 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 1326

L14 ANSWER 8 OF 13 USPATFULL on STN
AB A semiconductor device comprising a semiconductor body having a depression formed into the first surface of the body. The device further comprises member means comprising first and second thermal-to-electric transducer or static electric element, the member means having a predetermined configuration suspended over the depression. The member

means is connected to the first surface at least at one location, the depression opening to the first surface around at least a portion of the predetermined configuration. The depression provides substantial physical and thermal isolation between the elements and the semiconductor body. In this manner, an integrated semiconductor device provides an environment of substantial physical and thermal isolation between the transducer or element and the semiconductor body.

AN 87:67706 USPATFULL
TI Semiconductor device microstructure
IN Higashi, Robert E., Minneapolis, MN, United States
PA Honeywell Inc., Minneapolis, MN, United States (U.S. corporation)
PI US 4696188 19870929
AI US 1985-773106 19850906 (6)
RLI Continuation of Ser. No. US 1983-480644, filed on 31 Mar 1983, now abandoned which is a division of Ser. No. US 1981-310262, filed on 9 Oct 1981, now abandoned
DT Utility
FS Granted
EXNAM Primary Examiner: Goldstein, Herbert
LREP Mersereau, Charles G.
CLMN Number of Claims: 93
ECL Exemplary Claim: 1
DRWN 13 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 1528

L14 ANSWER 9 OF 13 USPATFULL on STN
AB A semiconductor device comprising a semiconductor body having a depression formed into the first surface of the body. The device further comprises a member comprising a thermal-to-electric transducer or static electric element or electrical-to-thermal element, the member having a predetermined configuration suspended over the depression. The member is connected to the first surface at least at one location, the depression opening to the first surface around at least a portion of the predetermined configuration. The depression provides substantial physical and thermal isolation between the element and the semiconductor body. In this manner, an integrated semiconductor device provides an environment of substantial physical and thermal isolation between the transducer or element and the semiconductor body.

AN 86:65560 USPATFULL
TI Semiconductor device
IN Johnson, Robert G., Minnetonka, MN, United States
Higashi, Robert E., Minneapolis, MN, United States
PA Honeywell Inc., Minneapolis, MN, United States (U.S. corporation)
PI US 4624137 19861125
AI US 1985-782197 19851001 (6)
RLI Continuation of Ser. No. US 1983-481095, filed on 31 Mar 1983, now abandoned which is a division of Ser. No. US 1981-310345, filed on 9 Oct 1981, now abandoned
DT Utility
FS Granted
EXNAM Primary Examiner: Goldstein, Herbert
LREP Mersereau, Charles G., Sumner, John P
CLMN Number of Claims: 90
ECL Exemplary Claim: 1
DRWN 13 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 1707

L14 ANSWER 10 OF 13 USPATFULL on STN
AB A semiconductor device comprising a semiconductor body having a depression formed into the first surface of the body. The device further comprises member means comprising a thermal-to-electric or static

electric element, the member means having a predetermined configuration suspended over the depression. The member means is connected to the first surface at least at one location, the depression opening to the first surface around at least a portion of the predetermined configuration. The depression provides substantial physical and thermal isolation between the element and the semiconductor body. In this manner, an integrated semiconductor device provides an environment of substantial physical and thermal isolation between the element and the semiconductor body.

AN 84:52568 USPATFULL
TI Method of making semiconductor device
IN Johnson, Robert G., Minnetonka, MN, United States
Higashi, Robert E., Minneapolis, MN, United States
PA Honeywell, Inc., Minneapolis, MN, United States (U.S. corporation)
PI US 4472239 19840918
AI US 1983-512079 19830708 (6)
RLI Division of Ser. No. US 1981-310345, filed on 9 Oct 1981
DT Utility
FS Granted
EXNAM Primary Examiner: Powell, William A.
LREP Sumner, John P.
CLMN Number of Claims: 8
ECL Exemplary Claim: 1
DRWN 13 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 1123

L14 ANSWER 11 OF 13 USPAT2 on STN
AB A method of manufacturing a ferrodielectric liquid crystal display device includes the steps of injecting melted ferrodielectric liquid crystal in a cell formed between a lower structure body and an upper structure body each having a substrate, an electrode layer, and an orientation film and sealing the cell; cooling to obtain phase transitions of the ferrodielectric liquid crystal corresponding to a bookshelf structure; applying dc potentials to the electrode layers at temperature ranging from temperatures higher than phase transition temperatures to temperatures lower than phase transition temperatures, stopping the dc potential applications and cooling until below a predetermined temperature, and applying a reverse potential to the electrode layers and cooling again. The ferrodielectric liquid crystal display device produced by such a manufacturing method can display clear black-and-white states with the liquid **crystal** layers having a **mono** domain of the bookshelf structure.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:11802 USPAT2
TI Ferrodielectric liquid crystal display (FLCD) manufacturing method
IN Wang, Jong-min, Seoul, KOREA, REPUBLIC OF
Kim, Chang-ju, Gyunggi-do, KOREA, REPUBLIC OF
PA Samsung Electronics Co., Ltd., Gyunggi-Do, KOREA, REPUBLIC OF (non-U.S. corporation)
PI US 6844909 B2 20050118
AI US 2003-403521 20030401 (10)
PRAI JP 2002-18086 20020402
DT Utility
FS GRANTED
EXNAM Primary Examiner: Nguyen, Dung T.; Assistant Examiner: Caley, Michael H
LREP Sughrue Mion, PLLC
CLMN Number of Claims: 5
ECL Exemplary Claim: 1
DRWN 8 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 435
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

09/681,715

Robert M. Bain
(314) 231-5400
117/14, 15, 201, 202, 204

10/623,967

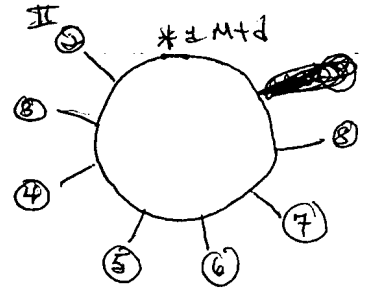
Examiner's Notes

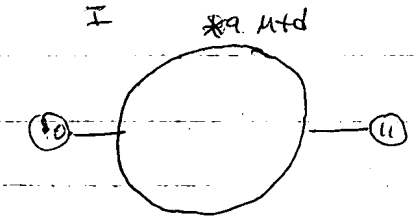
S(single or mono) (8a) (crystal?)
S(LPD or flow(w) pattern(w) defect# or COP or gate(w) oxide (w) integrite or COP or crystal (w) originated(w) particle or LPD or light(w) point(w) defect#
S(post(w) grow?) (10a) (process? or parameter# or rate#)
S(cool? (4a) rate#) (8a) (ingot# or boule# or crystal#)
S(without or wone or NO) (6a) (edge(w) slip#)
S(determin? or control?) (8a) (cool? (4a) rate#)
S(adjust? or vary! or control? or determin? or alter?) (10a) (post (4a) grow? or after (4a) grow?)
* Print Fig. 9 S(error(w) signal/#)

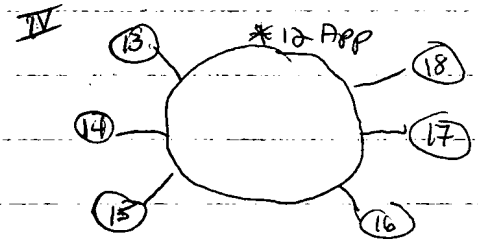
~~S(first~~
S(first or primary) (8a) (temperature (6a) sensor)
S(second) (8a) (temperature (6a) sensor)

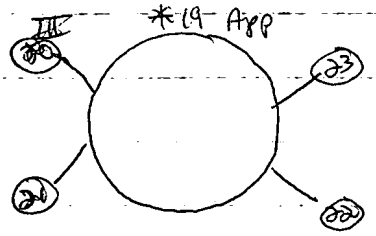
6,599,815
~~6,339,182~~
6,339,016

112¶2 Rej
Claim 1, line 2, "... czochralski process ..."
Claim 9, line 2, "... czochralski process ..."
Claim 12, line 2, "... CZ process ..."
Claim 19, line 2, "... CZ process ..."









L14 ANSWER 12 OF 13 USPAT2 on STN
AB A method and apparatus for axially growing single crystal silicon carbide is provided. Utilizing the system, silicon carbide can be grown with a dislocation density of less than 10.sup.4 per square centimeter, a micropipe density of less than 10 per square centimeter, and a secondary phase inclusion density of less than 10 per cubic centimeter. As disclosed, a SiC source and a SiC seed crystal of the desired polytype are co-located within a crucible, the growth zone being defined by the substantially parallel surfaces of the source and the seed in combination with the sidewalls of the crucible. Prior to reaching the growth temperature, the crucible is evacuated and sealed, either directly or through the use of a secondary container housing the crucible. The crucible is comprised of tantalum or niobium that has been specially treated. As a result of the treatment, the inner surfaces of the crucible exhibit a depth variable composition of Ta--Si--C or Nb--Si--C that is no longer capable of absorbing SiC vapors, thus allowing the vapor-phase composition within the crucible to be close to the SiC--Si system with the partial pressure of Si-vapor slightly higher than that in the SiC--Si system.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:162313 USPAT2
TI Tantalum crucible fabrication and treatment
IN Vodakov, Yury Alexandrovich, St. Petersburg, RUSSIAN FEDERATION
Mokhov, Evgeny Nikolaevich, St Petersburg, RUSSIAN FEDERATION
Ramm, Mark Grigorievich, Rego Park, NY, United States
Roenkov, Alexandr Dmitrievich, St. Petersburg, RUSSIAN FEDERATION
Makarov, Yury Nikolaevich, Richmond, VA, United States
Karpov, Sergei Yurievich, St. Petersburg, RUSSIAN FEDERATION
Ramm, Mark Spiridonovich, St Petersburg, RUSSIAN FEDERATION
Temkin, Leonid Iosifovich, St. Petersburg, RUSSIAN FEDERATION
PA The Fox Group, Inc., Livermore, CA, United States (U.S. corporation)
PI US 6547877 B2 20030415
AI US 2001-849767 20010504 (9)
RLI Continuation-in-part of Ser. No. US 355561, now patented, Pat. No. US 6261363
PRAI WO 1997-RU5 19970122
DT Utility
FS GRANTED
EXNAM Primary Examiner: Kunemund, Robert
LREP Bingham McCutchen, LLP, Beck, David G.
CLMN Number of Claims: 34
ECL Exemplary Claim: 1
DRWN 3 Drawing Figure(s); 1 Drawing Page(s)
LN.CNT 574
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L14 ANSWER 13 OF 13 USPAT2 on STN
AB A method and apparatus for axially growing single crystal silicon carbide is provided. Utilizing the system, silicon carbide can be grown with a dislocation density of less than 10.sup.4 per square centimeter, a micropipe density of less than 10 per square centimeter, and a secondary phase inclusion density of less than 10 per cubic centimeter. As disclosed, a SiC source and a SiC seed crystal of the desired polytype are co-located within a crucible, the growth zone being defined by the substantially parallel surfaces of the source and the seed in combination with the sidewalls of the crucible. Prior to reaching the growth temperature, the crucible is evacuated and sealed, either directly or through the use of a secondary container housing the crucible. The crucible is comprised of tantalum or niobium that has been specially treated. As a result of the treatment, the inner surfaces of the crucible exhibit a depth variable composition of Ta--Si--C or

Nb--Si--C that is no longer capable of absorbing SiC vapors, thus allowing the vapor-phase composition within the crucible to be close to the SiC--Si system with the partial pressure of Si-vapor slightly higher than that in the SiC--Si system.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:117934 USPAT2

TI Niobium crucible fabrication and treatment

IN Vodakov, Yury Alexandrovich, St. Petersburg, RUSSIAN FEDERATION
Mokhov, Evgeny Nikolaevich, St Petersburg, RUSSIAN FEDERATION
Ramm, Mark Grigorievich, Rego Park, NY, United States
Roenkov, Alexandr Dmitrievich, St. Petersburg, RUSSIAN FEDERATION
Makarov, Yury Nikolaevich, Richmond, VA, United States
Karpov, Sergei Yurievich, St. Petersburg, RUSSIAN FEDERATION
Ramm, Mark Spiridonovich, St Petersburg, RUSSIAN FEDERATION
Temkin, Leonid Iosifovich, St. Petersburg, RUSSIAN FEDERATION

PA The Fox Group, Inc., Livermore, CA, United States (U.S. corporation)

PI US 6537371 B2 20030325

AI US 2001-849766 20010504 (9)

RLI Continuation-in-part of Ser. No. US 355561, now patented, Pat. No. US 6261363

DT Utility

FS GRANTED

EXNAM Primary Examiner: Kunemund, Robert

LREP Bingham McCutchen, LLP, Beck, David G.

CLMN Number of Claims: 34

ECL Exemplary Claim: 1

DRWN 3 Drawing Figure(s); 1 Drawing Page(s)

LN.CNT 574

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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